Claims

What is claimed is:

[c1] A method for reducing a magnitude of a rate of current change for an integrated circuit, comprising:

determining when power consumption by the integrated circuit needs to be reduced; and

gradually reducing an amount of current sourced by a power supply based on the determination.

[c2] The method of claim 1, wherein gradually reducing the amount of current comprises:

selectively disabling a first transistor based on the determination, wherein disabling the first transistor causes a reduction in an amount of current sourced from a power supply; and

selectively disabling a second transistor based on the determination, wherein disabling the second transistor causes a reduction in the amount of current sourced from the power supply.

[c3] The method of claim 2, wherein the determination is made by a micro-architectural stage, the micro-architectural stage comprising:

selectively generating a signal to a counter stage, wherein the counter stage generates a first signal to the first transistor and a second signal to the second transistor.

[c4] The method of claim 3, wherein the counter stage comprises at least one selected from the group consisting of a finite state machine and a counter.

[c5] The method of claim 2, further comprising:

selectively disabling a last transistor based on the determination, wherein

disabling the last transistor causes a reduction in the amount of current sourced from the power supply.

[c6] The method of claim 5, wherein the determination is made by a micro-architectural stage, the micro-architectural stage comprising:

selectively generating a signal to a counter stage, wherein the counter stage generates a last signal to the last transistor.

[c7] The method of claim 5, wherein the counter stage comprises at least one selected from the group consisting of a finite state machine and a counter.

[c8] The method of claim 5, further comprising:

selectively enabling the first, second, and last transistors when power consumption by the integrated circuit does not need to be reduced.

[c9] The method of claim 5, wherein the first, second, and last transistor can each be one selected from the group consisting of a p-type transistor and a n-type transistor.

[c10] A method for reducing a magnitude of a rate of current change for an integrated circuit, comprising:

a step of determining when power consumption by the integrated circuit needs to be reduced; and

a step of gradually reducing an amount of current sourced by a power supply based on the determination.

[c11] The method of claim 10, wherein the step of gradually reducing the amount of current comprises:

a step of selectively disabling a first transistor based on the step of determining, wherein disabling the first transistor causes a reduction in an amount of current sourced from a power supply; and

a step of selectively disabling a second transistor based on the step of determining, wherein disabling the second transistor causes a reduction in an amount of current sourced from a power supply.

[c12] The method of claim 11, wherein the step of determining is made by a micro-architectural stage, the micro-architectural stage comprising:

a step of selectively generating a signal to a counter stage, wherein the counter stage generates a first signal to the first transistor and a second signal to the second transistor.

[c13] The method of claim 11, further comprising:

a step of selectively disabling a last transistor based on the step of determining, wherein disabling the last transistor causes a reduction in the amount of current sourced from the power supply.

[c14] The method of claim 11, wherein the step of determining is made by a micro-architectural stage, the micro-architectural stage comprising:

a step of selectively generating a signal to a counter stage, wherein the counter stage generates a last signal to the last transistor.

[c15] The method of claim 13, further comprising:

a step of selectively enabling the first, second, and last transistors when power consumption by the integrated circuit does not need to be reduced.